**In the Claims**

## CLAIMS

1. (Currently amended) A method of forming an isolation trench in a semiconductor material comprising:

forming a first isolation trench portion within a semiconductor material with a first gas mixture, the first isolation trench portion having a first depth within the semiconductor material and having a first sidewall intersecting a surface of the semiconductor material at a first angle;

forming a second isolation trench portion within the semiconductor material with a second gas mixture different from the first gas mixture, the second isolation trench portion being formed within and extending below the first isolation trench portion, the second isolation trench portion having a second depth within the semiconductor material and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle;

filling the first and second isolation trench portions with dielectric material; and

wherein the forming of the first isolation trench portion comprises forming the first isolation trench portion to have ~~having~~ a first depth of between five and ~~fifty~~ thirty percent of a sum of the first and second depths within the semiconductor material ~~total trench depth~~.

2. (Currently amended) The method of claim 1, wherein the forming of the ~~a~~ second isolation trench portion includes forming the second angle to be between eighty and ninety degrees.

3. (Currently amended) The method of claim 1, wherein the forming of the ~~a~~ first isolation trench portion includes forming the first angle to be in a range of from about thirty degrees to about seventy degrees and forming a second isolation trench portion includes forming the second angle to be more than eighty degrees.

4. (Currently amended) The method of claim 1, wherein the semiconductor material comprises silicon.

5. (Currently amended) A method of forming an isolation trench in a semiconductor material comprising:

forming a first isolation trench portion having a first depth within a semiconductor material and having a first sidewall intersecting a surface of the semiconductor material at a first angle;

forming a second isolation trench portion within and extending below the first isolation trench portion within the semiconductor material, the second isolation trench portion having a second depth within the semiconductor material and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle;

filling the first and second isolation trench portions with dielectric material;

wherein the forming of the first isolation trench portion comprises forming the first isolation trench portion to have ~~having~~ a first depth of between five and fifty percent of a sum of the first and second depths within the semiconductor material ~~total trench depth~~;

wherein the forming ~~a~~ of the first isolation trench portion comprises:

forming a silicon nitride layer ~~on~~ over the semiconductor material surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including masking layer sidewalls;

plasma etching through the silicon nitride layer using plasma conditions that also deposit a polymer on the masking layer sidewalls;

continuing the plasma etching for a predetermined time interval after the silicon nitride layer has been ~~broached~~ etched through and continuing to deposit

polymer on the masking layer sidewalls to form the first isolation trench portion using the same plasma conditions; and

stopping the plasma etching and the depositing ~~at the end of~~ when the predetermined time interval ends.

6. (Currently amended) The method of claim 5, wherein the plasma etching and the depositing ~~comprises~~ comprise:

providing a mixture of ~~gasses~~ gases chosen from a group consisting of $CF_4$, $CHF_3$, $CH_2F_2$ and $C_2F_8$; and

supplying radio frequency excitation to the mixture.

7. (Currently amended) The method of claim 5, wherein the plasma etching and the depositing ~~comprises~~ comprise:

providing a mixture of fluorocarbon gases; and

supplying radio frequency excitation to the mixture.

8. (Currently amended) The method of claim 1, wherein the forming of the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including $CF_4$ and $CHF_3$ in a ratio of ~~$CF_4/CHF_3 = 0.11$~~ $CF_4/CHF_3$ from 0.11 to 0.67.

Claims 9-10 (Canceled).

11. (Original) The method of claim 1, further comprising planarizing the dielectric material filling the first and second isolation trench portions.

12. (Currently Amended) The method of claim 1, wherein the forming of said first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

13. (Currently Amended) A method of forming an isolation trench ~~in~~ through a silicon surface of a silicon wafer comprising:

forming a mask ~~on~~ over the silicon surface, the mask including ~~an~~ a mask opening and mask sidewalls; and

etching through the silicon surface into the silicon wafer using gases including $CF_4$ and $CHF_3$ in a ratio of ~~$CF_4/CHF_3 = 0.11$~~ $CF_4/CHF_3$ from 0.11 to 0.67 to form a first isolation trench portion, wherein the etching forms the opening and sidewalls in the mask.

14. (Currently Amended) The method of claim 13, wherein the etching of the silicon surface includes forming said first isolation trench portion having a first sidewall that intersects the silicon surface at an angle in a range of from about thirty degrees to about seventy degrees.

15. (Currently Amended) The method of claim 14, wherein the forming of said first isolation trench portion comprises forming said first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

16. (Currently amended) The method of claim 13, further comprising forming a second isolation trench portion within the silicon wafer and extending below the first isolation trench portion, the second isolation trench portion including a second sidewall intersecting the first sidewall at an angle with respect to the silicon surface that is greater than the first angle.

17. (Currently Amended) The method of claim 16, wherein the forming of said first isolation trench portion comprises forming said first isolation trench portion having a first depth within the silicon wafer of between five and fifty percent of a sum of the first and second depths within the silicon wafer ~~total trench depth~~.

18. (Currently amended) The method of claim 17, further comprising:

filling the first and second isolation trench portions with dielectric material; and

planarizing the dielectric material ~~filling~~ within the first and second isolation trench portions.

19. (Currently amended) The method of claim 13, wherein the forming ~~a~~ of the mask comprises:

forming a silicon nitride layer on the ~~semiconductor~~ silicon surface; and

forming ~~a~~ another masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

Claim 20 (Cancelled).

21. (Currently amended) The method of claim 19, further comprising forming a second isolation trench portion within the silicon wafer and extending below the first isolation trench portion, the second isolation trench portion having a second depth within the silicon wafer and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle.

22. (Currently amended) A method of forming an isolation trench-isolated transistor comprising:

forming first and second isolation trenches disposed to a respective side of a portion of silicon, the forming the first and second isolation trenches comprising:

forming a mask on ~~the~~ a surface of the portion of silicon, the mask including first and second openings corresponding to the first and second isolation trenches;

forming a first isolation trench portion within the portion of silicon in each of the first and second openings, each first isolation trench portion having a first depth within the portion of silicon and having a first sidewall intersecting a surface of the ~~semiconductor~~ portion of silicon at a first angle; and

forming a second isolation trench portion within the portion of silicon and extending below each of the first isolation trench portions, the second isolation trench portions having a second depth within the portion of silicon and including a second sidewall intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater than the first angle, the second isolation trench portion having a bottom portion of silicon at the second depth;

doping the bottom portion of the second isolation trench portion;

the method further comprising:

filling the first and second isolation trench portions with dielectric material;

forming a gate extending across the ~~silicon portion~~ portion of silicon from the first isolation trench to the second isolation trench; and

forming source and drain regions within the portion of silicon and extending between the first and second isolation trench portions, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

23. (Currently amended) The method of claim 22, wherein the forming of said first isolation trench portion comprises etching the silicon surface using gases including $CF_4$ and $CHF_3$ in a ratio of ~~$CF_4/CHF_3 = 0.11$~~ $CF_4/CHF_3$ from 0.11 to 0.67.

24. (Currently amended) The method of claim 22, wherein the forming ~~a~~ of the mask comprises:

forming a silicon nitride layer ~~on~~ over the ~~semiconductor~~ silicon surface; and

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

25. (Currently amended) A method of forming an isolation trench-isolated transistor comprising:

forming first and second isolation trenches disposed to a respective side of a portion of silicon, the forming the first and second isolation trenches comprising:

forming ~~a mask on~~ an oxide layer over the surface of the portion of silicon, the oxide layer including first and second openings corresponding to the first and second isolation trenches;

forming a first isolation trench portion within the portion of silicon in each of the first and second openings, each first isolation trench portion having a first depth within the portion of silicon and having a first sidewall intersecting a surface of the ~~semiconductor~~ portion of silicon at a first angle; and

forming a second isolation trench portion within the portion of silicon and extending below each of the first isolation trench portions, the second isolation trench portions having a second depth within the portion of silicon and including a second sidewall intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater than the first angle; the method further comprising:

filling the first and second isolation trench portions with dielectric material;

forming a gate extending across the silicon portion from the first isolation trench to the second isolation trench;

forming source and drain regions within the portion of silicon and extending between the first and second isolation trench portions, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

wherein forming a first isolation trench portion comprises:

plasma etching through the ~~silicon nitride~~ oxide layer using plasma conditions that also deposit a polymer on the sidewalls;

continuing plasma etching for a predetermined time after the ~~silicon nitride~~ oxide layer has been broached and continuing to deposit polymer on the sidewalls to form the first isolation trench portion using the same plasma conditions; and

stopping the etching and depositing at the end of the predetermined interval.

26. (Currently amended) The method of claim 25, wherein the plasma etching comprises etching using gases including $CF_4$ and $CHF_3$ in a ratio of ~~$CF_4/CHF_3 = 0.11$~~ $CF_4/CHF_3$ from 0.11 to 0.67.

27. (Currently amended) The method of claim 22, wherein the forming of said first isolation trench portion comprises forming said first isolation trench portion having a first sidewall intersecting a surface of the ~~semiconductor~~ portion of silicon at an angle in a range of from about thirty degrees to about seventy degrees.

28. (Currently amended) The method of claim 22, wherein the forming of said ~~a~~ first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

29. (Currently amended) The method of claim 27, wherein the forming ~~a~~ of the second isolation trench portion comprises forming a second isolation trench portion having a second sidewall forming an angle of more than eighty degrees with the surface.

30. (Currently amended) The method of claim 22, wherein the forming ~~a~~ of the first isolation trench portion comprises forming ~~a~~ the first isolation trench portion having a first depth of between five and fifty percent of a sum of the first and second depths within the portion of silicon ~~total trench depth~~.

31. (Original) The method of claim 30, further comprising planarizing the dielectric material filling the first and second isolation trench portions.

32. (Previously presented) The method of claim 22, wherein the gate comprises polysilicon.

Claims 33-61 (Canceled).

62. (Previously presented) The method of claim 22 wherein the source region is disposed adjacent only one side of the gate.

63. (Previously presented) The method of claim 22 wherein the drain region is disposed adjacent only one side of the gate.

64. (Previously presented) The method of claim 22 wherein the source region and drain region are disposed directly opposite one another on opposite sides of the gate.

65. (Currently amended) A method of forming an isolation trench in a semiconductor material comprising:

forming a first isolation trench portion within a semiconductor material having a first depth within a semiconductor material and having a first sidewall intersecting a surface of the semiconductor material at a first angle;

forming a second isolation trench portion within a semiconductor material and extending below the first isolation trench portion, the second isolation trench portion having a second depth within a semiconductor material and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle;

filling the first and second isolation trench portions with dielectric material;

wherein the forming of the first isolation trench portion comprises:

forming a silicon nitride layer on the semiconductor material surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including masking layer sidewalls;

plasma etching through the silicon nitride layer using plasma conditions that also deposit a polymer on the masking layer sidewalls, the plasma conditions comprising a mixture of gases chosen from a group consisting of $CF_4$, $CHF_3$, $CH_2F_2$ and $C_2F_8$;

continuing the plasma etching for a predetermined time interval after the silicon nitride layer has been ~~broached~~ etched through and continuing to deposit polymer on the masking layer sidewalls to form the first isolation trench portion using the same plasma conditions; and

stopping the plasma etching and the depositing ~~at the end of~~ when the predetermined time interval ends.

66. (Currently amended) The method of claim 65, wherein the plasma etching and the depositing ~~comprises~~ comprise:

~~providing a mixture of gasses chosen from a group consisting of $CF_4$, $CHF_3$, $CH_2F_2$ and $C_2F_8$; and~~

supplying radio frequency excitation to the mixture.

Claims 67-68 (Canceled).

69. (New) A method of forming an isolation trench in a semiconductor substrate comprising:

forming a masking layer over a semiconductor substrate;

etching through the masking layer and exposing an upper surface of the semiconductor substrate, the etching comprising over-etching through the upper surface of the semiconductor substrate while some of the masking layer masks some of the substrate to form a first isolation trench portion within the semiconductor substrate, the first isolation trench portion having a first depth within the semiconductor substrate and having a first sidewall intersecting the upper surface of the semiconductor substrate at a first angle;

forming a second isolation trench portion within the semiconductor substrate, the second isolation trench portion being formed within and extending below the first isolation trench portion, the second isolation trench portion having a second depth within the semiconductor substrate and including a second sidewall intersecting the first sidewall at an angle with respect to the upper surface that is greater than the first angle; and

filling the first and second isolation trench portions with dielectric material.

70. (New) The method of claim 69, wherein the masking layer comprises a silicon nitride layer.

71. (New) The method of claim 69, wherein the masking layer comprises an oxide layer.

72. (New) The method of claim 69, wherein the etching comprises an environment of etch gases with respective ratios of component gases, and wherein the over-etching comprises the same etch gases in different respective ratios of the component gases.

73. (New) The method of claim 69, wherein the over-etching comprises an environment of etch gases, and wherein the forming of the second isolation trench portion comprises a different environment of different etch gases.

74. (New) The method of claim 69 further comprising:

terminating the forming of the second isolation trench portion; and

de-chucking the semiconductor substrate in an environment of argon.

75. (New) The method of claim 69, wherein the etching and the over-etching comprises a plasma environment of etch gases.

76. (New) The method of claim 69, wherein the etching and the over-etching comprises an environment of at least $CF_4$, $CHF_3$ and argon.

77. (New) The method of claim 69, wherein the etching comprises an environment of at least $CF_4$ and $CHF_3$ gases, and wherein the over-etching comprises varying at least one of the gases.

78. (New) The method of claim 69, wherein the etching comprises an environment of at least $CF_4$ and $CHF_3$ gases, and wherein the over-etching comprises varying at least the $CF_4$ and $CHF_3$ gases.

79. (New) A method of forming an isolation trench in a semiconductor substrate comprising:

forming a masking layer over a semiconductor substrate;

etching through the masking layer and exposing an upper surface of the semiconductor substrate, the etching comprising an environment of etch gases with respective ratios of component gases;

etching through the upper surface of the semiconductor substrate to form a first isolation trench portion within the semiconductor substrate, the etching comprising the environment of the same etch gases and the same respective ratios of the component gases, the first isolation trench portion having a first depth within the semiconductor substrate and having a first sidewall intersecting the upper surface of the semiconductor substrate at a first angle;

etching a second isolation trench portion within the semiconductor substrate, the second isolation trench portion being formed within and extending below the first isolation trench portion, the second isolation trench portion having a second depth within the semiconductor substrate and including a second sidewall intersecting the first sidewall at an angle with respect to the upper surface that is greater than the first angle; and

filling the first and second isolation trench portions with dielectric material.

80. (New) The method of claim 79, wherein the etch gases of the environment comprise at least $CF_4$, $CHF_3$ and argon.